EE431\_01

MOS-based 555 Timer

Industry Summary

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December 7, 2021

**Abstract**

This project started off as an exploration of the propagation delay for the 555 timer, to which it switched many times until our Cadence License constraint pushed us towards CMOS-based 555 timer. This paper covers our team’s attempt to push through a sufficient device on a chip within our time constraint.

**Exploration**

With our supervising instructor, Professor Tina Smilkstein, we considered going for a faster 555 timer, however, Dr. Smilkstein pointed out the limiting factor being the external capacitor’s RC constant rather than the circuit design itself in the pursuit of optimizing the propagation delay. This led to some research on a sinc-wave generator that was possible, however, the blocks necessary within this process relied on our colleagues finishing their parts in time to be able to use their adders, multipliers, and even timers themselves to be able to create a sine wave from a summing amplifier that would superposition delayed square waves, followed by a multiplying circuit to form a digitally recognizable sinc function, hopefully enough to fool a digital input with the product of the two resultant sine waves of differing frequencies.

This ended up being not a particularly do-able project, and with the deadline cutting close, we switched back to the 555 timer. Based on some brief research, the comparator seemed promising in changing the performance of a 555 timer, but relative to modern applications, a 555 is outdated and grants particular hobbyist interest in modernizing its design.

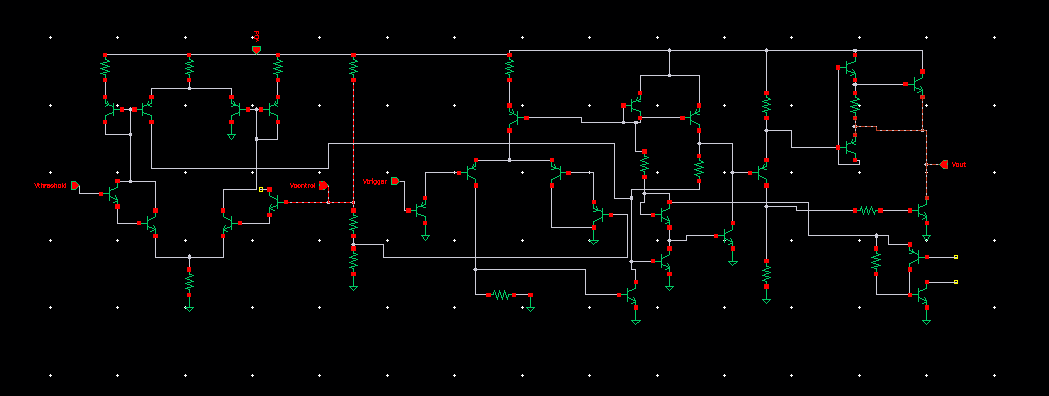


Figure 1. Our Working and Dysfunctional 55 timer

After successfully making a test threshold comparator, we went on to add the trigger comparator, flip flop, and output stage with its reset circuit in Figure 1. The timing signal had a 1.5VDC offset with a rather small amplitude, but the timing was correct, and before going on to troubleshoot, we encountered an impasse.

Our design in Cadence wouldn’t be able to work with an incomplete bjt model library from TSMC’s 180nm process, so we had to switch to a MOS-based 555 timer.

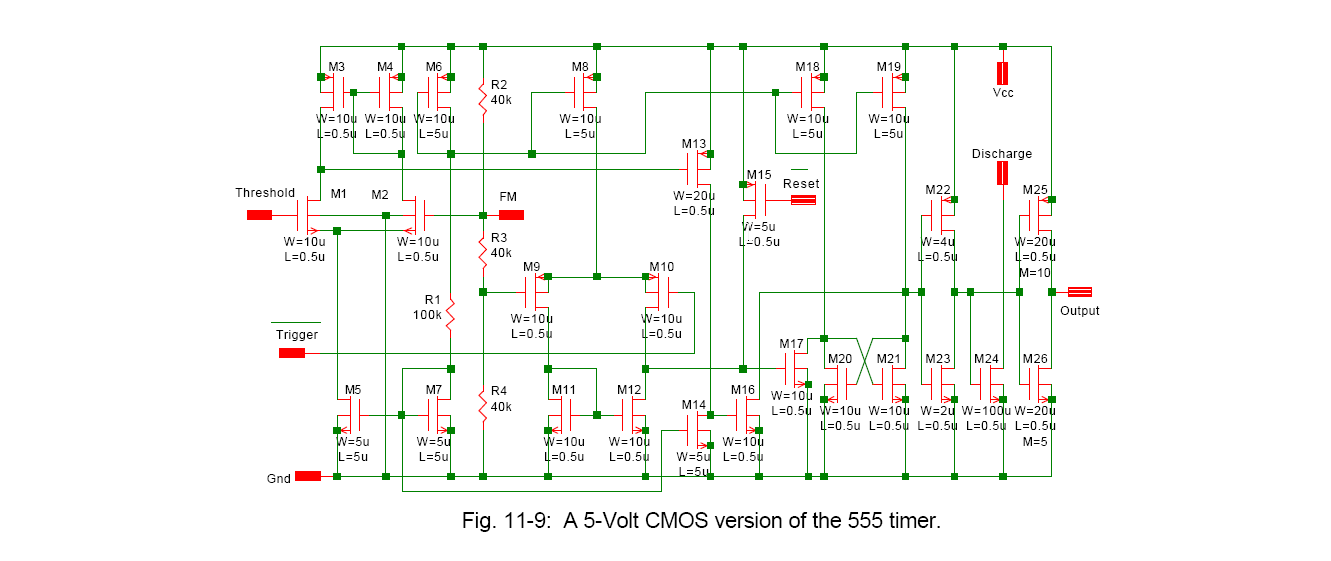


Figure x. Desired MOS-based 555 Timer

**Simulation**

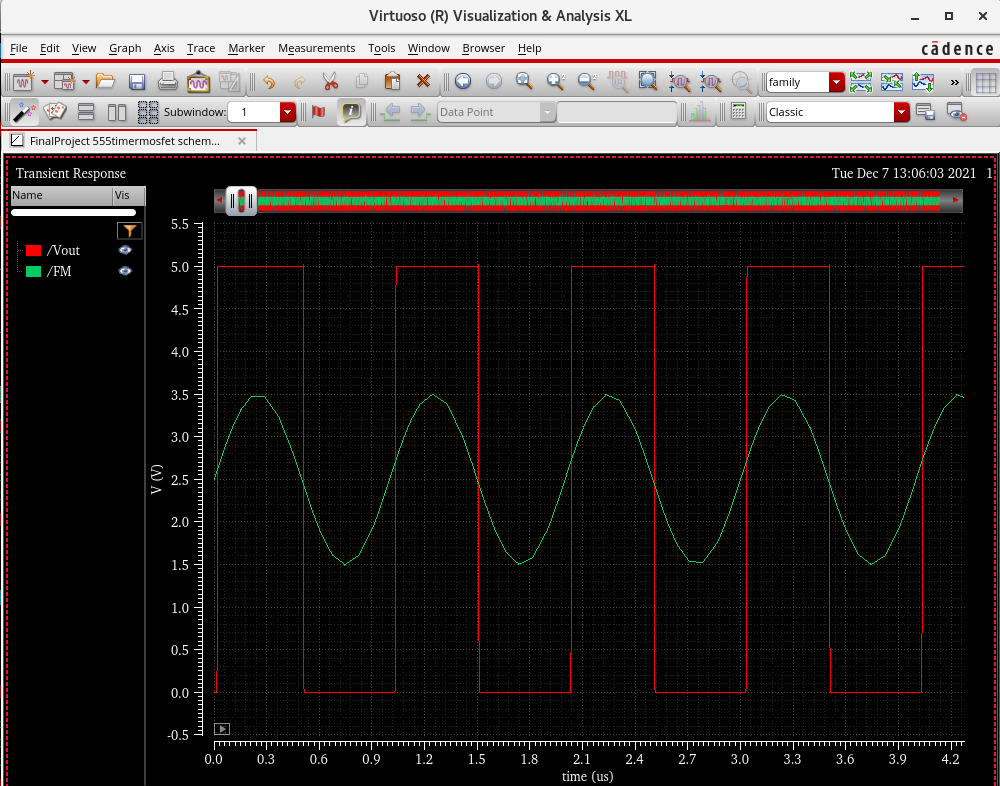


Figure 2. Simulated MOS-based 555 Timer

The MOS-based 555 timer worked splendidly.

Parameters for Sim:

* VDD = 5V
* Vin or FM = Sine wave (2.5VDC, 2.5VAC, 1MHz)
* VThreshold = 2.5V
* VTrigger = 1.25V
* Ignored: Reset, Discharge

**Layout**

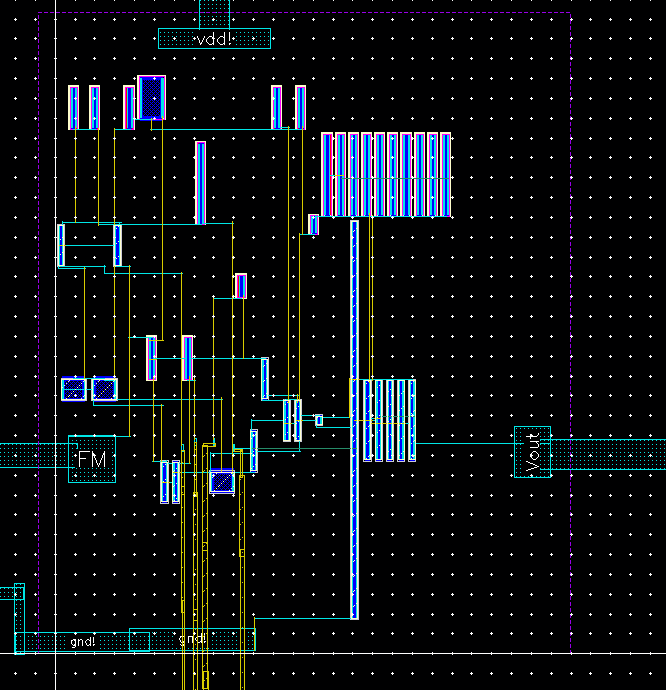


Figure 3. Layout Design in Cadence’s Virtuoso of our MOS-based 555 Timer

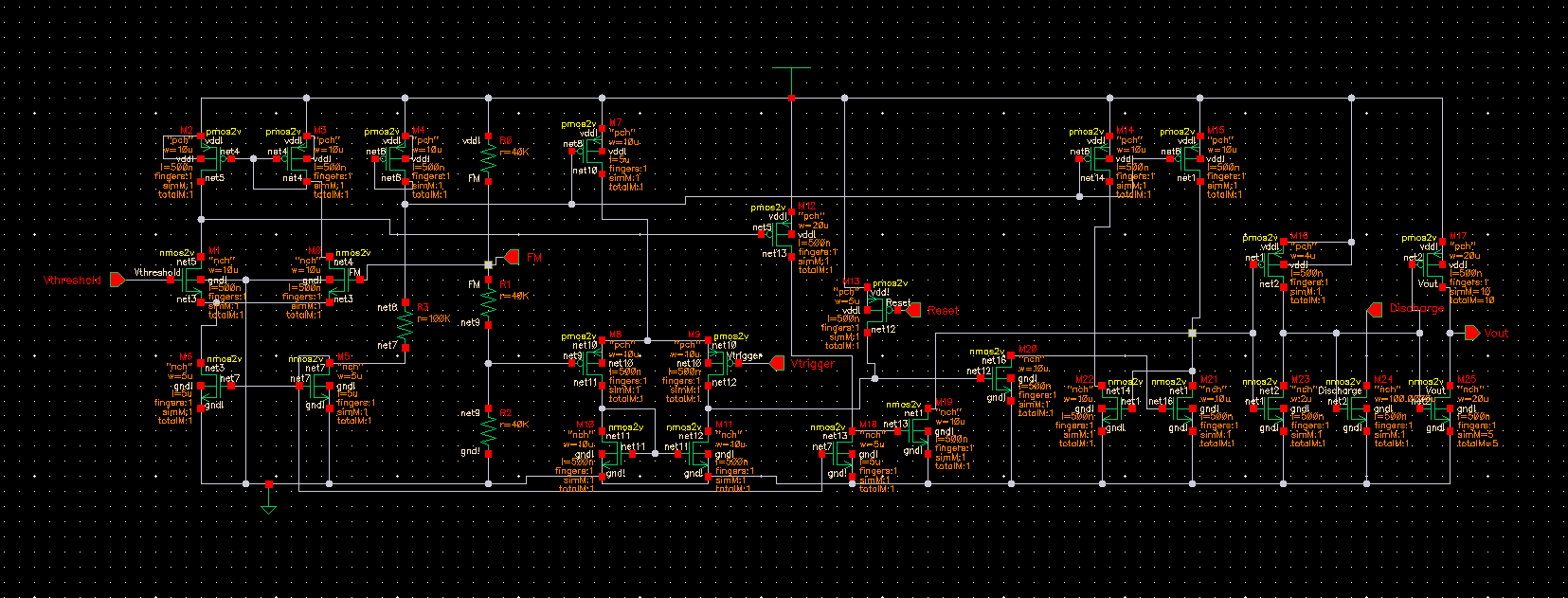


Figure 4. Schematic in Cadence’s Virtuoso of our MOS-based 555 Timer

**Layout with IO Pads**

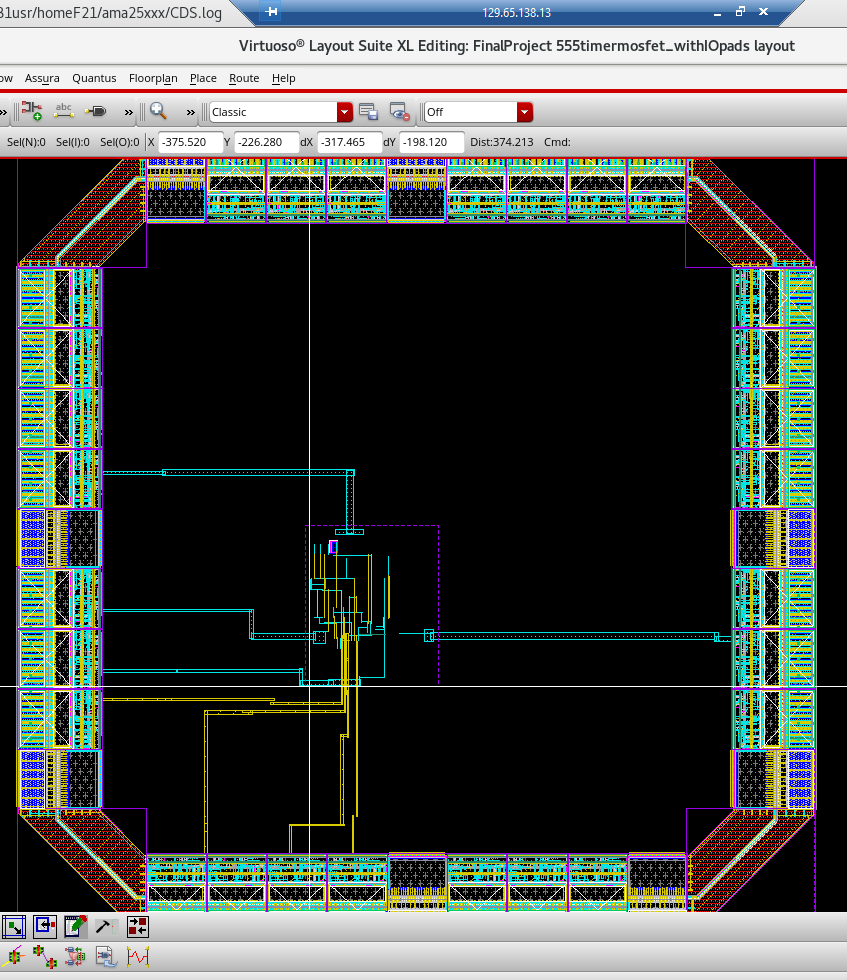


Figure 5. Layout with IO Pads in Cadence’s Virtuoso of our MOS-based 555 Timer

**Potential Applications**

There were an incredible number of roadblocks, not including ourselves, what remains is a finishing blurb on the possibilities for our design.

The TSMC 180nm process is manufactured with a 2V power rating for the supply rails, a 5V supply rail would surely cause immediate cracks in the fingers, metals, and vias very quickly. So there are two possibilities: design parts with 5V power ratings or create a 2V timer with 5V output capabilities with an additional external output stage.

The 555 timer is already an outdated component for modern uses, but this lends to the possibility of using our newly gained MOS-based timer design experience to create our own modern-ready timer with mosfets with a different conceptual premise.